PVP 14

Code: CS2T4

I B.Tech - II Semester - Regular / Supplementary Examinations – May 2017

DIGITAL LOGIC DESIGN
(COMPUTER SCIENCE & ENGINEERING)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks

11x 2 = 22 M

1.

a) Convert 1101101 to Octal and Hexadecimal Number.
b) Convert 395.18 to binary and hexadecimal numbers.
c) Implement AB+A'B' using only NOR gates.
d) What is don't care condition? How to represent in K-Map?
e) Simplify the following expression.
   ABC+A'B+AB'C+ABC'
f) What is Look Ahead Carry adder?
g) Compare ROM, PAL and PLA.
h) Compare Asynchronous and Synchronous Counters.
i) What is the difference between latch and flip-flop?
j) What are applications of flip-flops?
k) Define decoder and encoder.

PART – B

Answer any ***THREE*** questions. All questions carry equal marks.

3 x 16 = 48 M

2. a) Perform Subtraction with the following unsigned decimal numbers by taking 10's complement of the subtrahend

   i) 20-100
   ii) 1200-250
   iii) 1753-8640
   iv) 5250-1321

   8 M

   b) Represent the following decimal numbers in BCD 13597, 93286 and 99880. 8 M

3. a) Design a 2-bit Magnitude Comparator. 8 M

   b) Simplify the SOP form using a 4 variable K-Map
   $F(A,B,C,D) = \sum(0,2,4,8) + d(3,5)$ 8 M

4. a) Design a combinational circuit binary to gray code Converter. 8 M

   b) Design a half adder circuit. 8 M

5. a) Design a Decade Counter using D-Flip-Flop. 8 M

   b) Compare combinational and sequential circuits. 8 M

6. Design a PAL circuit using following Boolean Functions

   $W(A,B,C,D) = \sum(2,12,13)$

   $X(A,B,C,D) = \sum(7,8,9,10,11,12,13,14,15)$

   $Y(A,B,C,D) = \sum(0,2,3,4,5,6,7,8,10,11,15)$

   $Z(A,B,C,D) = \sum(1,2,8,12,13)$ 16 M